**Design Verification**

Semiconductor industry is growing worldwide in a rapid pace, and creating jobs in large number. But the shortage of skilled and well trained resources becomes a problem for such a growth in India. Our certification course DVE is structured to fill the gap that exist between the fresh graduates from colleges and the industry in terms of technical and soft skill requirements. Typically, a VLSI verification engineer verifies the functionality and performance compliance of a design with respect to specifications and ensures that designs are correct. A verification engineer is required to develop a verification environment which mimics the real world deployment scenario also known as Verification Intellectual Property (VIP) for the design under test (DUT) and also captures the failure models for the design. This training course includes soft skill development programs, industry expert's talk and projects on industry standard projects, in addition to the interactive classroom sessions from working professionals.

**Module 1:**

**Introduction to VLSI**

Application of VLSI

Design Process of VLSI

Scope of VLSI

Introduction to VLSI Design flow

**Module 2:**

**Digital Electronics**

Number Systems - Review

Logic Minimization

Combinational Circuit Design

Understanding of a Logic Gate

Designing with Mux, Demux, Decoders, Encoders

Sequential Elements - D Latch, D Flop

Design of Sequential Systems - Registers and Counters

Finite State Machine

**Module 3:**

**Introduction to HDL**

History of Hard ware design

Benefits of HDL

HDL basics

Data Types and Operators

**HDL Programming**

Procedural and Continuous Assignments

Control flow statements

Blocking v/s Non-Blocking

Tasks and Functions

FSM Coding

Synthesizable Design

**Module 4:**

**System Verilog**

Compile Directive

System Tasks

File Management

OOP in System Verilog

Verilog Event Scheduling

Interface and Clocking

Process Synchronization

Program Blocks and Parameter

Functional Coverage

System Verilog Assertions

**Module 5:**

**UVM**

UVM Architecture

UVC Sequence items and Sequences

Basic concepts

Messaging

Stimulus Generation

Virtual Sequences

Virtual Sequencer

Communication between components

Drivers

Sequencers

Monitors

Subscribers

**Module 6:**

**Transaction Level Modelling (TLM)**

Concepts and Terminology

Simple uni-directional interfaces (put, get, peek)

More complex connections (transport, analysis)

TLM FIFOs and analysis FIFOs

Hierarchical connections with export

Analysis

**Module 7:**

**Register Layer**

Register layer architecture and features

Front door and back door access

Mirroring and updating

Address maps

Register adapters

Integrating registers into the environment

Register sequences

Built-in register test sequences

**Module 8:**

System Verilog and UVM Based Verification IP Project